ABSTRACT

An architecture and process for forming CMOS vertical replacement gate metal oxide semiconductor field-effect transistors is disclosed. The integrated circuit structure includes a semiconductor area with a major surface formed along a plane and first and second source/drain dopes regions formed in the surface. An insulating trench is formed between the first and second source/drain regions. A third doped region forming a channel of a different conductivity type than the first source/drain region is positioned over the first source/drain region. A fourth doped region is formed over the second source/drain region, having an opposite conductivity type with respect to the second source/drain region, and forming a channel region. Fifth and sixth source/drain regions are formed respectively over the third and fourth doped regions.

In an associated method of manufacturing the semiconductor device, first and second source/drain regions are formed in the semiconductor layer, followed by the formation of third and fourth doped regions forming the channel. Fifth and sixth doped regions are then formed over the channels to complete the structure. An insulating region is formed between the first and the second source/drain regions to isolate these regions of opposite conductivity type.